AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (previously presented): A semiconductor package board comprising:

a metal base plate having an opening suited for receiving therein a semiconductor chip; and

a multilayer wiring film formed on said metal base plate;

said multilayer wiring film having a first surface, said first surface having a first region in contact with said metal base plate, said first surface having a second region exposed by said opening in said metal base plate; and

a plurality of first metal pads formed in said second region.

2. (original): The semiconductor package board according to claim 1, wherein said multilayer wiring film includes a plurality of wiring layers and a plurality of insulating layers alternately stacked upon one another, via holes formed in said plurality of insulating layers for interconnecting said plurality of wiring layers, and a plurality of second metal pads formed on a second surface of said multilayer wiring film opposite to said first surface, and wherein said second metal pads are electrically connected to said first metal pads through said wiring layers and said via holes.

3. (original): The semiconductor package board according to claim 1, wherein said multilayer wiring film has a metallic film in contact with a periphery of said opening of said metal base plate.

4. (original): The semiconductor package board according to claim 1, wherein said multilayer wiring film mounts thereon a thin-film capacitor between at least one of said first metal pads and said wiring layers.

5. (original): The semiconductor package board according to claim 1, wherein said metal base plate comprises at least one metal selected from the group consisting of stainless steel, iron, nickel, copper, and aluminum, or an alloy thereof.

6. (original): The semiconductor package board according to claim 1, wherein said first metal pads are covered by a surface layer comprising at least one metal selected from the group consisting of gold, tin, and solder, or an alloy thereof.

7. (original): The semiconductor package board according to claim 2, wherein each of said insulating layers comprises one or more of organic resins selected from the group

consisting of an epoxy resin, an epoxy acrylate resin, an urethan acrylate resin, a polyester resin, a phenol resin, a polyimide resin, a benzocyclobutene (BCB), and a polybenzoxazole (PBO).

8. (original): The semiconductor package board according to claim 2, further comprising a carrier base mounted on said second surface of said multilayer wiring film and connected to said second metal pads.

9 (original): The semiconductor package board according to claim 8, wherein said carrier base is connected to said second metal pads either through conductive paste or through an anisotropic conductive film.

10. (original): The semiconductor package board according to claim 8, wherein said carrier base is one of printed circuit board, ceramic board, and organic/inorganic composite board, having at least one wiring layer.

11. (original): The semiconductor package board according to claim 8, wherein said carrier base includes a resistor.

12. (original): The semiconductor package board according to claim 8, wherein said carrier base includes a capacitor.

13. (original): The semiconductor package board according to claim 8, wherein said carrier base is electrically connected to ground.

14. (original): The semiconductor package board according to claim 8, wherein said carrier base mounts thereon a plurality of either solder balls or connector pins on a surface thereof opposite to a surface in contact with said multilayer wiring film, said solder balls or connector pins being electrically connected to said second metal pads through said carrier base.

15. (original): A semiconductor device comprising the semiconductor package board according to claim 1, and a semiconductor chip disposed within said opening and connected to said first metal pads.

16. (original): The semiconductor device according to claim 15, wherein said semiconductor chip is flip-chip bonded to said first metal pads by a material made of either a metal having a low melting point or a conductive resin.

17. (original): The semiconductor device according to claim 15, wherein said semiconductor chip is connected to said multilayer wiring film by at least one material selected from the group consisting of a metal having a low melting point, an organic resin, and a resin containing a metal.

Claims 18-41 (canceled).

42. (previously presented): The semiconductor package board according to claim 1, wherein said first metal pads comprise a surface, a portion of said surface is not in direct contact with said multilayer wiring film, said portion being coplanar with said multilayer wiring film.

43. (previously presented): The semiconductor package board according to claim 1, wherein said first metal pads comprise a surface, a portion of said surface is not in direct contact with said multilayer wiring film, said portion being recessed toward said first surface of said multilayer wiring film.

44. (previously presented): The semiconductor package board according to claim 1, wherein the surface of said first metal pads is recessed from the surface of said multilayer wiring film.

45. (previously presented) A semiconductor package board comprising:

a metal base plate having an opening; and

a multilayer wiring film formed on said metal base plate, said multilayer wiring film having a first surface in contact with said metal base plate and mounting thereon a plurality of first metal pads within a region exposed from said opening of said metal base plate, wherein surface of the first metal pads is recessed form the surface of the multilayer wiring film.

46. (new): The semiconductor package board according to claim 1, wherein said multilayer wiring film is formed directly on said metal base plate.

47. (new): The semiconductor package board according to claim 42, wherein said portion of said surface of said first metal pads is flat.

48. (new): The semiconductor package board according to claim 43, wherein said portion of said surface of said first metal pads is flat.

49. (new): The semiconductor package board according to claim 43, wherein

said multilayer wiring film comprises a recess corresponding to said portion of said surface of said first metal pads recessed toward said first surface of said multilayer wiring, and

said recess has the same dimensions as said portion of said surface of said first metal pads when viewed in a direction perpendicular to said portion of said surface of said first metal pads.